REMARKS

Applicant wishes to thank the Examiner for the attention accorded to the instant application, and respectfully requests reconsideration of the application as amended.

Formal Matters

In this Response, claim 1 is amended to incorporate the limitations of claim 2, and claim 2 is canceled. Claims 27 and 28 are amended to more clearly recite the invention; support for these amendments can be found in the specification on page 41, lines 1-10. Claims 38-40 are added. Support for these new claims can be found in the specification on page 20, lines 13-18, and on page 19, lines 22-24. No new matter has been added.

Applicant respectfully requests that the Examiner review and consider the references cited in the Information Disclosure Statement (IDS) filed on February 24, 2004 with the application, as well as the IDS filed January 11, 2006, and the IDS filed April 24, 2006.

Specification

In the specification, the following paragraphs have been amended to make minor editorial corrections: the paragraph beginning on page 6, line 7, the paragraph beginning on page 11, line 12; the paragraph beginning on page 19, line 18, the paragraph beginning on page 26, line 7, the paragraph beginning on page 29, line 22, the paragraph beginning on page 35, line 7, and the paragraph beginning on page 43, line 25.

Claim Objections

Claims 27 and 28 are objected to because it appears that "pipeline" should be "pipeline stage". Applicant amends claims 27 and 28 to change "pipeline" to "pipeline stage". Withdrawal of this objection is respectfully requested.

Rejection of Claims Under 35 U.S.C. §102

Claim 9 is rejected under 35 U.S.C. § 102(b) as anticipated by Hammond, et al., U.S. Patent No. 5,774,686 (hereinafter "Hammond"). This rejection should be withdrawn based on the comments and remarks herein.

Among the problems recognized and solved by Applicant's claimed invention is the need for a processor in which, even if there is an increase in the number of instruction sets to be switched among, there is no increase in the size of the decoder circuitry for decoding an instruction-set changeover instruction. Further, in applicant's inventive solution, insertion of the changeover instruction can easily be performed because it is unnecessary to recognize an instruction set that prevailed prior to changeover. In one embodiment, applicant's inventive processor can have a pipeline control architecture that is capable of switching between an instruction set and a number of pipeline stages of every instruction set.

The Examiner contends that Hammond's disclosure of a multiple step process of translating instructions, decoding the translated instructions, and executing the decoded instructions (column 15, lines 47-57) teaches a processor having a pipeline control architecture and comprising a unit for receiving a stage-number setting instruction and a unit for setting variably the number of stages in the pipeline control in response to the received stage-number setting instruction. Applicant respectfully disagrees.

Hammond discloses a processor that can switch between instruction set architectures and system architectures (column 4, lines 36-37), but does not disclose or suggest any specific system architecture. Further, Hammond discloses that one decoder 830 can be replaced with a translator, that the translator's output can be used as input to the other decoder 835 which can output to the execution unit 840. Hence, Hammond discloses a series of rigid steps performed

one after the other, that is, the second step requires input from the first step and the third step requires the input from the second step. Accordingly, Hammond discloses a fixed procedure, not a variable number of stages. Because the procedure of Hammond is fixed, Hammond does not disclose or suggest setting *variably* the number of stages in a pipeline control architecture in response to the received stage-number setting instruction, as recited in claim 9. Thus, Hammond does not disclose or suggest each feature of claim 9.

It has been held by the courts that "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GMBH v. American Hoist and Derrick Company et al.*, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984). As illustrated above, Hammond does not disclose either stage-number setting instructions or setting variably the number of stages in a pipeline control architecture and hence does not disclose each and every feature of the invention as recited in independent claim 9, so that it is patentable over the art of record in the application. Therefore, withdrawal of this rejection is kindly requested.

Rejection of Claims 1-4, 6-8, 21-37 Under 35 U.S.C. §103

Claims 1-4, 6-8 and 21-37 are rejected under 35 U.S.C. § 103(a) as unpatentable over Hammond in view of Trivedi, et al., U.S. Patent No. 6,430,674 (hereinafter "Trivedi"). This rejection should be withdrawn based on the comments and remarks herein.

The Examiner asserts that Hammond fails to disclose a decoder used exclusively for the switch instruction. However, claim 1 recites "a system instruction decoder, *provided separately of the plurality of processor functions*, for decoding a system instruction not executed by any of the plurality of processor functions". Applicant respectfully states that the Examiner's interpretation of the claim language is too narrow. The claims are interpreted in light of the

specification, which states "The system instruction that specifies the instruction set used is executed using the system decoder and system instruction execution unit that are exclusively for the system instruction." (see *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)). No particular "switch instruction" is disclosed or recited in the claims of the present invention. Thus the invention is not limited to having a specific "switch instruction" but instead merely recites "a system instruction not executed by any of the plurality of processor functions".

The Examiner asserts that Trivedi discloses a decoder used exclusively for the switch instruction. Applicant respectfully disagrees. Trivedi discloses a detector that can detect the presence of a mode switch instruction in the decoder (column 4, lines 24-26). Trivedi further discloses multiple decoders, one for each instruction set (column 4, lines 2-24). The multiple decoders of Trivedi decode instructions into fixed length microcode that are then executed (column 4, lines 28-31, emphasis added). However, Trivedi does not disclose or suggest "a system instruction decoder, provided separately of the plurality of processor functions, for decoding a system instruction *not executed* by any of the plurality of processor functions" as recited in claim 1. Thus claim 1 is patentably distinguishable over the art of record in the application. Claims 2-4 and 6-8 depend from claim 1, incorporating all of the features and limitations of the base claim. Accordingly, claims 2-4 and 6-8 are patentably distinguishable over the art of record in the application for at least the reasons that claim 1 is patentably distinguishable over the art of record in the application.

Regarding independent claim 21, as discussed above, Trivedi discloses a decoder 302b and a detector 306 which can detect the presence of a mode switch instruction in the decoder. Trivedi does not disclose or suggest a system instruction decoder receiving a predetermined system instruction. Thus, the hypothetical combination of Hammond and Trivedi does not

disclose or suggest each feature of independent claim 21, so that claim 21 is patentably distinguishable from the art of record in the application. Claim 22 depends from claim 21, incorporating all of the features and limitations of the base claim. Accordingly, claim 22 is patentably distinguishable over the art of record in the application for at least the reasons that claim 21 is patentably distinguishable over the art of record in the application.

Further, the Examiner asserts that Hammond discloses a first processing unit that executes processing based on only a first decoded result among a first decoded result and a second decoded result, and a common processor unit that executes processing based on both the first and second decoded results, as recited in independent claim 23. Applicant respectfully disagrees.

Hammond discloses an execution unit 840 to execute the decoded instructions from both instruction sets (column 14, lines 11-14). No other processing units are disclosed. Further, Hammond discloses that the register file 850 stores the values related to the x86 instruction set and is accessed by the execution unit 840 based on the instructions in the 64-bit instruction set, and therefore the register unit 850 does not execute processing based on only the decoded results of the x86 instruction set (column 14, lines 14-35, Figure 8). In addition, the register file 855 stores the values related to the 64-bit instruction set and is accessed by the execution unit 840 based on the instructions in the x86 instruction set, and therefore the register file 855 does not execute processing based on only the decoded results of the 64-bit instruction set. Hence, Hammond merely discloses that the execution unit 840 is used regardless of the instruction set, while the register files 850, 855 are used separately, one for each instruction set. Consequently, Hammond does not disclose both a first processing unit that executes processing based only on a

first decoded result, and a common processing unit that executes processing based on both the first and second decoded results, as recited in claim 23.

Trivedi does not overcome this deficiency and the Examiner does not state otherwise. Thus, the hypothetical combination of Hammond and Trivedi does not disclose each and every feature recited in independent claim 23, so that claim 23 is patentably distinguishable from the art of record in the application. It has been held by the courts that to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. See, *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). As illustrated above, the hypothetical combination of Hammond and Trivedi lacks a first processing unit that executes processing based only on a first decoded result, and a common processing unit that executes processing based on both the first and second decoded results. Hence this hypothetical combination does not disclose or suggest each and every feature of the present invention as recited in independent claim 23. Thus *prima facie* obviousness has not been established. Accordingly, claim 23 is distinguishable over the art of record in the application. Claims 24-37 depend from claim 23, incorporating all of the features and limitations in claim 23. Hence, claims 24-37 are patentably distinguishable from the art of record in the application for at least the reasons that claim 23 is patentably distinguishable from the art of record in the application. Accordingly, withdrawal of this rejection is requested.

Rejection of Claim 5 Under 35 U.S.C. §103

Claim 5 is rejected under 35 U.S.C. § 103(a) as unpatentable over Hammond in view of Trivedi, in view of Dalvi, U.S. Patent No. 6,167,529. This rejection should be withdrawn based on the comments and remarks herein.

As discussed above, neither Hammond nor Trivedi disclose a system instruction decoder for decoding a system instruction as recited in claim 1. Dalvi does not overcome this deficiency, and the Examiner does not state otherwise. Thus independent claim 1 is patentably distinguishable from the art of record in the application. Claim 5 depends from claim 1, incorporating all of the features of its base claim. Hence, claim 5 is patentable over the art of record in the application for at least the reasons that its base claim is patentable over the art of record. Accordingly, this rejection should be withdrawn.

Rejection of Claims 10-12 Under 35 U.S.C. §103

Claims 10-12 are rejected under 35 U.S.C. § 103(a) as unpatentable over Hammond in view of Glass, U.S. Patent No. 5,774,686. This rejection should be withdrawn based on the comments and remarks herein.

As discussed above, Hammond does not disclose or suggest each and every feature in independent claim 9. In particular, Hammond lacks a stage-number setting instruction and setting variably the number of stages in a pipeline control architecture in response to the received stage-number setting instruction. Glass does not overcome this deficiency, and the Examiner does not state otherwise. Thus independent claim 9 is patentably distinguishable from the art of record in the application. Claims 10-12 depend from claim 9, each dependent claim incorporating all of the features of its base claim. Hence, claims 10-12 are patentable over the art of record in the application for at least the reasons that their base claim is patentable over the art of record. Accordingly, this rejection should be withdrawn.

Conclusion

For at least the reasons set forth in the foregoing discussion, Applicant believes that the Application is now allowable, and respectfully requests that the Examiner reconsider the rejection and allow the Application. Should the Examiner have any questions regarding this Amendment, or regarding the Application generally, the Examiner is invited to telephone the undersigned attorney.

Respectfully submitted,

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